REMARKS

The Office Action dated December 1, 2005 in this Application has been carefully considered. Claims 1-23 and 25-29 are pending. The above amendments and the following remarks are presented in a sincere attempt to place this Application in condition for allowance. Claims 11, 25-26, and 28-29 have been amended in this Response. Claim 24 has been cancelled in this Response. Claims 1-23 have been determined by the Examiner to be in condition for the allowance. Applicant thanks the Examiner. Reconsideration and allowance are respectfully requested in light of the above amendments and following remarks for those Claims not in condition for allowance.

Applicants wish to thank the Examiner for the courtesy of the interview conducted on February 16, 2006. During the interview, the above-referenced amendments were discussed.

The Examiner has indicated that Claims 1-23 are in condition for allowance. *See* Office Action, Page 1. Applicants thank the Examiner. Additionally, Claim 11 has been amended in this response to correct a minor typographical error.

The Examiner has indicated that Claims 25 and 29 would be allowable if rewritten or amended to overcome the rejections under 35 U.S.C. §112, second paragraph, as described below. *See* Office Action, Page 3. Accordingly, Claims 25 and 29 have been amended to stand in independent form and to address the Examiner's rejections.

In particular, Claims 24-29 stand rejected under 35 U.S.C. §112, second paragraph, as allegedly being "indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention." Office Action, Page 2. Applicants respectfully traverse these rejections.

Regarding Claim 24, the Examiner stated, "Claim 24 appears to be misdescriptive since 'reset means' and 'second logic means' limitations are recited for 'resetting of each of said downstream divider trees' wherein figure 6 of the instant application shows only 'second logic means' being capable of doing so." Office Action, Page 2. Claim 24 has been cancelled in this Response. However, Claim 25 has been amended in this Response to recite the limitations of Claim 24, putting Claim 25 in independent form. Accordingly, Claim 25 has also been amended to address the Examiner's rejection of Claim 24 under 35 U.S.C. §112, second paragraph. Specifically, Claim 25, as amended, now recites, in relevant part, "second logic means, connected to first logic means and said reset means, for receiving said first logic means indication and for determining a proper clock cycle at which to issue a signal to the reset means, *wherein the reset means is configured for providing the synchronous divider reset signal in response to the received signal from the second logic means.*" (Emphasis added). Accordingly, Applicants respectfully request that this rejection be withdrawn.

Regarding Claim 25, the Examiner stated, "the limitation 'a sampling latch', line 5, appears to refer to a first logic means as recited in claim 24 since element 402 in figure 4 is the only element which receives *the first and second clocks* (as required by claim 24) and *receives an output of the delay element* (as required by claim 25). Office Action, Page 2 (emphasis in original). Applicants respectfully point out that Claim 25 recites, "wherein *the first logic means* further comprises: a delay element . . . and a sampling latch." (Emphasis added). Thus, Claim 25 expressly recites the first logic means as comprising a sampling latch. Applicants therefore respectfully request that this rejection be withdrawn and that Claim 25 be allowed.

Regarding Claim 26, the Examiner stated that, "the limitation 'the asynchronous divider reset signal' lacks antecedent basis." Office Action, Page 2. Claim 26 has been amended in this

Response to depend from Claim 25 and to recite, in relevant part, "wherein the reset means further comprises a plurality of *synchronization* latches, wherein at least one latch of the plurality of *synchronization* latches is at least configured to receive *an* asynchronous divider reset signal, and wherein at least one synchronization latch of the plurality of synchronization latches is at least configured to produce a sync signal." (Emphasis added). Applicants therefore respectfully request that this rejection be withdrawn and that Claim 26 be allowed.

Regarding Claims 27-29, the Examiner rejected these Claims as "being dependent on the rejected claims as noted above." Office Action, Page 2. Claim 26 has been amended in this response to depend from allowed Claim 25. Claim 27 depends from Claim 26. Claim 28 has been amended in this response to depend from allowed Claim 25. Claim 29 has been re-written in independent form including the limitations of intervening Claims, to recite, in relevant part, "second logic means, connected to first logic means and said reset means, for receiving said first logic means indication and for determining a proper clock cycle at which to issue a signal to the reset means, *wherein the reset means is configured for providing the synchronous divider reset signal in response to the received signal from the second logic means.*" (Emphasis added). Accordingly, Applicants respectfully request that the rejections of Claims 27-29 be withdrawn and that Claims 27-29 be allowed.

Claims 24 and 26-28 stand rejected under 35 U.S.C. §102(b) by U.S. Patent No. 6,175,603 by Chapman et al. ("Chapman"). Insofar as they may be applied against the Claims, Applicants respectfully traverse these rejections.

Regarding Claim 24, Chapman was cited as assertedly fully disclosing the following:

(1) "in figure 2 an apparatus comprising first logic means 34 for indicating misaligned of first and second clocks (TICK_N and CLOCK_N)";

(2) "reset means 36 and 37, connected to said first logic means, for providing a synchronous divider reset signal (i.e., output of 40) for resetting each of said downstream divider trees (elements 24-26 as shown in figure 1 by way of element 40)"; and

(3) "second logic means 38, connected to first logic means and said reset, for receiving said first logic means indication and for determining a proper clock cycle at which to issue a signal to the reset means as required by claim 24." Office Action, Page 3.

Regarding Claim 26, the Examiner stated, "elements 36 and 37 are seen as a plurality of latches wherein element 36 receives an asynchronous divider reset signal SYS_CLK and element 37 produces a sync signal." Office Action, Page 3. Regarding Claim 27, the Examiner stated, "elements 36 and 37 in figure 2 are seen as a plurality of cascade flip-flops" and "[i]t is noted that AND logic gate is constructed by D-flip-flops." Office Action, Page 3. Regarding Claim 28, the Examiner stated, "element 40 is seen as a counting circuit as required by claim." Office Action, Page 3.

Claim 24 has been cancelled in this Response. Claim 26 has been amended to depend from allowed Claim 25. Claim 27 depends from Claim 26. Claim 28 has been amended to depend from allowed Claim 25. Accordingly, Applicants respectfully request that the rejection of Claims 26-28 under 35 U.S.C. § 102(b) be withdrawn and that Claims 26-28 be allowed.

Applicants have now made an earnest attempt to place this Application in condition for allowance. For the foregoing reasons and for other reasons clearly apparent, Applicants respectfully request full allowance of Claims 1-23 and 25-29.

Applicant encloses a check in the amount of $400.00 for two independent claims in excess of three. Applicants do not believe that any other fees are due; however, in the event that any other fees are due, the Commissioner is hereby authorized to charge any required fees due (other than issue fees), and to credit any overpayment made, in connection with the filing of this paper to Deposit Account No. 50-0605 of CARR LLP.

Should the Examiner deem that any further amendment is desirable to place this application in condition for allowance, the Examiner is invited to telephone the undersigned at the number listed below.

Respectfully submitted,

CARR LLP

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